Jehkaran Singh

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Education

B.Tech, Electronics and Computer Engineering — ***UPES Dehradun, India***
CGPA: **8.7/10.0** — **July 2023 – June 2027**
Relevant Coursework: VLSI Technologies, Digital Design, Embedded Systems

Electronics Engineering Technician (Diploma) — ***Seneca College, Canada***
CGPA: **3.0/4.0** — **Jan 2022 – Aug 2023**
Capstone: Automatic Security Switch – Designed an ESP32-based IoT power switching system.

Technical Skills

- **Hardware Design & HDL:** Verilog, VHDL, RTL Design, FSMs, Pipelining, Timing Analysis, CDC, AXI-Lite, MMIO
- **SoC & Verification:** SystemVerilog, Testbenches, Directed Simulation, ModelSim, Functional Verification
- **Embedded & Firmware:** Embedded C, Bare-Metal Programming, FreeRTOS, SPI/UART Protocols
- **EDA Tools & Software:** Vivado, ModelSim, MATLAB, Altium, Python, Git, Linux CLI, VS Code

Projects

- **RISC-V CPU with Custom AES ISA Extension** *(in progress)*
  Pipelined RV32I in **Verilog**; custom **AES** instruction with SubBytes/ShiftRows/MixColumns **datapath** in execute stage; **UART** plaintext-to-ciphertext demo on **FPGA**.
  Arch: 5-stage (IF/ID/EX/MEM/WB), **hazard detection + forwarding unit**; AES in R-type format with dedicated **combinational crypto datapath** bypassing ALU.

- **AXI-Lite Hardware Accelerator with Firmware Control**
  AXI-Lite slave, **register file**, **control FSM**, **datapath**; **synthesized** in Vivado, verified via directed **testbenches**; driven by **bare-metal firmware** on **FPGA**.
  Impl: **MMIO** address decode; FSM: IDLE→EXEC→DONE; firmware polls status register for completion.

- **Multichannel Signal Processing System** *(in progress)*
  3-channel **round-robin SPI ADC** pipeline; per-channel **AXI-Lite** accelerators for **FIR filtering**; on-fabric **DSP algorithms** for **edge computing** without host dependency.
  Arch: Arbitrated **SPI master** → dedicated **FIR** blocks → central **DSP core** via **AXI-Lite** fabric.

- **FPGA-Based Optical Sensor Acquisition System**
  Mixed-signal **FPGA** pipeline: **SPI** ADC master, **synchronous FIFO**, **UART** tx in **Verilog RTL**; deterministic 1 kHz streaming.
  Impl: 16-deep **FIFO** decouples acquisition/UART domains; **CDC** via gray-coded pointers; verified with **ModelSim** directed testbench.

Professional Experience

Shoppers Drug Mart, Assistant Manager, Toronto, Canada — **Jan 2022 – Aug 2024**
- Earned **Employee of the Month for 8 consecutive months** by exceeding operational and service KPIs.
- Streamlined inventory tracking and replenishment using **ERP/SAP systems**, reducing stock shortages by **30%** and completing **95%** of deadlines ahead of schedule.
- Trained and mentored **10+ staff** on POS, ERP, and internal systems, improving process adherence by **˜25%**.

Loblaws Inc., Co-op Technician Intern, Toronto, Canada — **Jan 2023 – Aug 2023**
- Diagnosed and resolved **150+ hardware, software, and network issues**, maintaining **99% system uptime** and cutting recurring issue resolution time by **40%**.
- Used **Wireshark, Visio, and CRM tools** to analyze faults, document root causes, and improve delivery efficiency by **15%**.

Certifications

- **ISWDP Level 1** – Samsung, IISc & Synopsys SARA Semiconductor Device Technology, TCAD-Based Design Workflow, 2D Device Simulation & Analysis. Scored **88%**
- **Control Systems Fundamentals** – Siemens
- **ERP Systems Training** – Shoppers Drug Mart